STT-MRAM Compute-In-Memory Ising Solver with Intrinsic Annealing for Large-Scale Combinatorial Optimization Problems

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Combinatorial optimization problems (COPs) are hard to solve efficiently on conventional CPUs because their search space grows exponentially with problem size. An Ising machine tackles these problems by mapping each variable to a spin and finding the spin pattern that minimizes the Ising Hamiltonian through annealing with dedicated hardware accelerators. We present a 16 nm compute-in-memory (CIM) Ising solver design that uses a standard foundry's STT-MRAM array and supports solving large-scale traveling salesman problems (TSPs) with complex constraints through hierarchical clustering and dense mapping. At each iteration, the spins are broadcast to the array; an analog CIM operation inside the MRAM array evaluates the change in Hamiltonian energy in a single access; and the result drives the next spin update. This architecture fits large problems (>2k spins) into a compact footprint of around 0.05mm^2. Stochastic MTJ switching under weak programming naturally supplies the random behavior required for simulated annealing, eliminating external random-number hardware while matching a target probability curve. The reliability of the design is verified through Monte Carlo simulations under various process–voltage–temperature (PVT) corners, and approximate solutions achieve ~115% distance of the algorithm baseline for a 96-city TSP. With MRAM's high density, low-power analog evaluation, and built-in stochasticity for annealing, the proposed macro offers an efficient hardware platform with competitive figure of merits including time-to-solution of 2ms and a >17x improvement in hardware cost ratio (defined as chip area/problem scale/precision).

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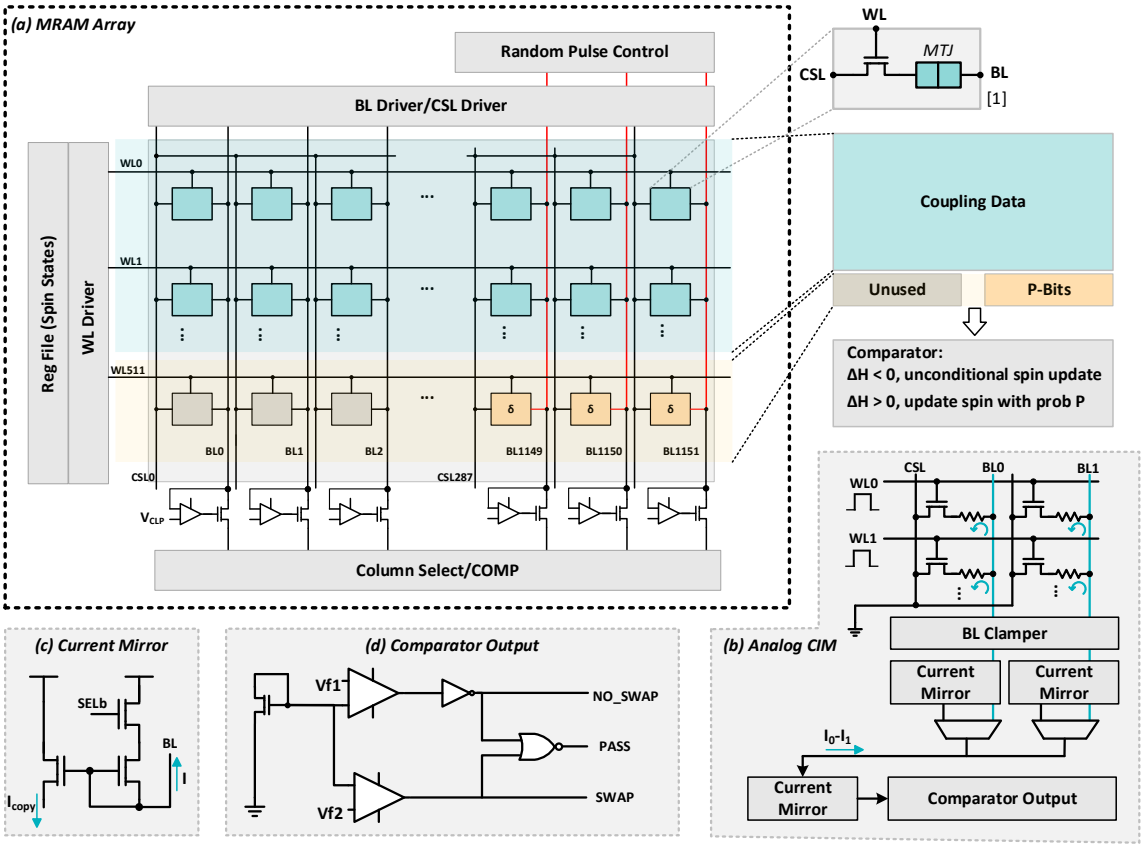

Fig. 1. (a) Block diagram of the MRAM array. (b) Illustration of the analog CIM and the current flow. (c) Schematic of current mirror. (d) Comparator output converts current to voltage and produces digital output.

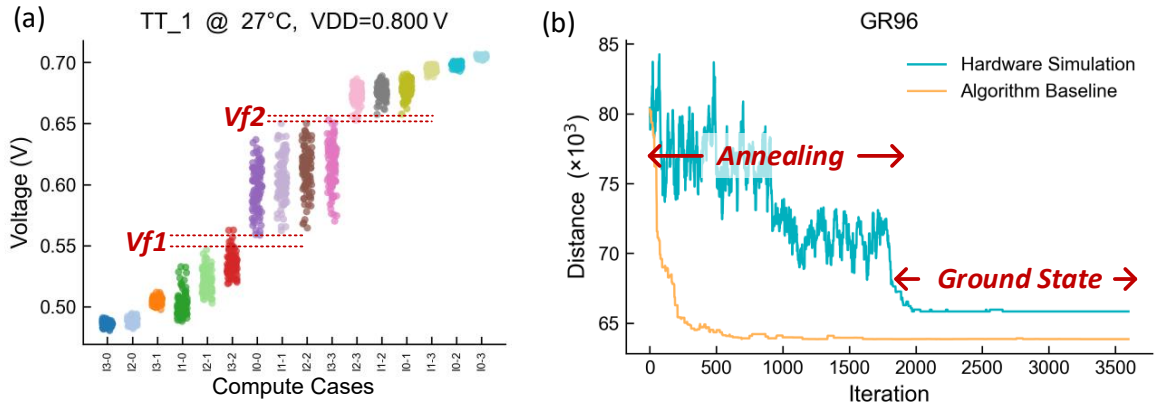

Fig. 2. (a) Monte Carlo simulation result showing the voltage distribution of each compute case with MTJ resistance variation. (b) Distance over iteration plot demonstrates Hamiltonian energy lowering using GR96 dataset, with final distance settles in ground state.

References

[1] K.-F. Lin et al., "15.9 A 16nm 16Mb Embedded STT-MRAM with a 20ns Write Time, a 1012 Write Endurance and Integrated Margin-Expansion Schemes," in 2024 IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2024, pp. 292–294.